## REJECTION UNDER 35 U.S.C. § 103

Claims 1-2, 5-8 and 12-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al (U.S. Pat. No. 5,970,384) in view of Grill et al (U.S. App. No. 2002/0037442 A1) and Yamazaki et al (U.S. App. No. 2002/0034863 A1). This rejection is respectfully traversed.

Claims 1, 7, 15, and 16 call for a method for the fabrication of a field-effect transistor comprising the steps of forming a semiconductor layer serving as an active layer on a substrate, setting the substrate temperature at no higher than 100°C, and forming a gate insulating film on the semiconductor layer.

The Examiner alleges that Yamazaki ('384) teaches a method for the fabrication of a field-effect transistor comprising the steps of forming a semiconductor layer, forming a stage gate insulating film on the semiconductor layer, and heat treating the gas insulating film. Yamazaki ('384) fails to teach setting the substrate temperature at no higher than 100°C and heat-treating the gate insulating film in an atmosphere containing water. However, the Examiner alleges that it would have been obvious to combine Grill's ('442) teaching of setting a substrate temperature between about 25°C and about 400°C and Yamazaki's ('863) teaching of heat treating in an atmosphere of water with the teaching of Yamazaki ('384) to arrive at the claimed invention.

Applicants respectfully assert, however, that the Examiner is not considering the references as a whole, is picking and choosing among the teachings of the references, and is using impermissible hindsight reasoning. Further, Applicants respectfully assert that the references do not suggest the desirability and thus the obviousness of making

the proposed combination. In fact, the references teach away from the claimed invention. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)

Despite teaching certain field-effect transistor fabrication steps, Yamazaki ('384) is not combinable with the remaining references. Yamazaki ('384) discloses in column 13, lines 2-8 that, "The TEOS which had been vaporized in a vaporizer and oxygen were introduced into a chamber which had parallel plate-type electrodes, RF power (for example, frequency 13.56 MHz) was introduced and a plasma was formed, and the accumulation was made at a substrate temperature of 200 – 500°C, and preferably of 250 – 400°C." (emphasis added)

By teaching that substrate temperature should be in the range of 200 – 500°C, Yamazaki ('384) directly teaches away from the claimed temperature of no higher than 100°C. The Examiner cannot pick and choose from among Yamazaki's ('384) teachings. One skilled in the art would not employ Yamazaki's ('384) fabrication steps in the present invention since the required substrate temperature is well above the claimed range.

Yamazaki ('384) must be considered as a whole. Yamazaki's ('384) teachings regarding substrate temperature cannot be discarded or ignored. One cannot arbitrarily change one aspect of Yamazaki's ('384) teachings, for example, temperature, and expect predictable results. As such, the teachings of Yamazaki ('384) are not properly combinable with the teachings of Grill ('442) and Yamazaki ('863). Further, even if the

proposed combination were made, the claimed invention would not result since the temperature taught by Grill ('442) would likely render Yamazaki ('384) inoperable.

Furthermore, Applicants respectfully assert that Yamazaki ('863) also teaches away from the claimed invention and that it would not have been obvious to combine Yamazaki's ('863) teaching of heat treating in an atmosphere of water with the teachings of Yamazaki ('384). Yamazaki ('863) in paragraph [0269] teaches that, "Heat treatment is then performed in a temperature range of from 500 to 700°C. This temperature range is set so that a thermal oxide film can be formed without generating any deformation or warping on the glass substrate." Yamazaki ('863) also directly teaches away from the claimed substrate temperature of no higher than 100°C. Yamazaki's ('863) teachings with respect to an atmosphere of water cannot be read in isolation. One must also consider that Yamazaki ('863) requires a temperature range of 500-700°C. By teaching a temperature of 500 to 700°C, one skilled in the art would believe that such a high temperature would be necessary to utilize the disclosed heat treating atmosphere containing water.

Only when one has the benefit of the claimed invention can one appreciate the proposed modification of Yamazaki ('384) to include the atmosphere containing water of Yamazaki ('863). This is impermissible hindsight reasoning. Since both Yamazaki ('384) and Yamazaki ('863) both teach away from the claimed invention, Applicants respectfully assert that one skilled in the art would not find the desirability and thus, the obviousness of making the proposed combination.

With respect to Grill ('442), Applicants respectfully assert that Grill's ('442) disclosed temperature condition of between about 25°C and about 400°C is not one that

is suitable to create a gate insulation layer, but is rather a temperature range used in a method of making a multiphase material with a low dielectric constant comprised of two precursors. Grill ('442) discloses in paragraph [0018] molecules suitable for the first precursor while molecules suitable for the second precursor are disclosed in paragraph [0019].

Moreover, Grill ('442) provides no suggestion that the disclosed temperature range would be desirable to use in combination with the claimed fabrication steps, the fabrication steps of Yamazaki ('384), or the atmosphere of water of Yamazaki ('863). Grill ('442) simply provides a broad statement in paragraph [0022] that, "The deposition of the multiphase material of this invention may further include the steps of setting the substrate temperature at between about 25°C and about 400°C..." Nowhere in the disclosure of Grill ('442), however, is there any reason or specific evidence why such a temperature range was chosen or its applicability to gate insulation layers. Grill's ('442) teachings with respect to temperature cannot be read out of context. Such teachings must be consider in conjunction with the remaining teachings of Grill ('442). When Grill is read as a whole, one skilled in the art does not find any motivation to utilize the teachings of Grill ('442) in combination with Yamazaki ('384) and Yamazaki ('863). Furthermore, it is doubtful that such a combination would be made since Yamazaki ('384) and Yamazaki ('863) teach directly away from such a temperature range.

In conclusion, neither Yamazaki ('384), Yamazaki ('863), nor Grill ('442) provides any motivation or suggestion that the proposed combination would be desirable. Both Yamazaki ('384) and Yamazaki ('863) teach away from the claimed invention by teaching temperatures far in excess of the claimed substrate temperature (no higher

than 100°C). Grill ('442) provides a broad temperature range, but provides no specific evidence for the chosen range or its applicability to the claimed fabrication steps. As such, there is no suggestion or motivation to combine the references cited, and therefore, reconsideration and withdrawal of this rejection is respectfully requested.

With respect to dependent claims 2, 5, 6, 8, and 12-14, Applicant believes these claims should be in condition for allowance for at least the same reasons as their independent base claims.

Claims 3-4 and 9-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al (U.S. Pat. No. 5,970,384), Grill et al (U.S. App. No. 2002/0037442 A1) and Yamazaki et al (U.S. App. No. 2002/0034863 A1) as applied to claims 1 and 7-8 above, and further in view of An et al (U.S. Pat. No. 6,245,618 B1). This rejection is respectfully traversed.

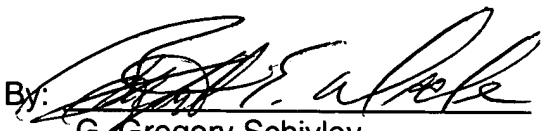
Claims 3-4 and 9-11 are dependent on independent claims 1 and 7, respectively. These claims should be in condition for allowance for at least the same reasons as set forth above.

## CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: September 26, 2002

By: 

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## ATTACHMENT FOR SPECIFICATION AMENDMENTS

The following is a marked up version of the title in which underlines indicates insertions and brackets indicate deletions.

"METHOD FOR FABRICATION OF FIELD-EFFECT TRANSISTOR TO REDUCE DEFECTS AT MOS INTERFACES FORMED AT LOW TEMPERATURE"